AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-37. (cancelled)

38. (previously presented A testing circuit comprising:

m (m is an integer of 2 or more) block test units, each of which compares a first data of n (n is a positive integer) bits with a reference data of said n bits for each corresponding bit, and outputs a comparison result as a test circuit output signal based on a output control signal, wherein said first data is outputted from corresponding one of m object circuits for a test; and

a first logical processing unit which judges whether or not said all of m said test circuit output signals indicate that said first data is coincident with said reference data, and outputs a judgment result as a total judgment result signal based on said m test circuit output signals,

wherein each of said m block test units includes:

a block judging unit which compares said first data with said reference data for each corresponding bit to judge whether said first data is coincident with said reference data, and outputs a comparison result as a block judgment result signal, and

a block output selecting unit which outputs one of said block judgment result signal and a predetermined standard signal as said test circuit output signal based on said output control signal.

39. (previously presented) The testing circuit according to claim 38, wherein said output control signal is set such that said block output selecting unit outputs one of said block judgment result signal and said standard signal, in reference to a test condition for said one of m object circuits when said first data is outputted.

40. (previously presented) The testing circuit according to claim 39, wherein said block output selecting unit outputs said block judgment result signal when said test condition corresponds to said one of m object circuits, and outputs said standard signal when test condition does not correspond to said one of m object circuits, based on said output control signal.

41. (previously presented) The testing circuit according to claim 39, wherein said standard signal is set as the same logical state of said block judgment result signal indicating that said first data is coincident with said reference data.

42. (previously presented) The testing circuit according to claim 38, wherein said total judgment result signal indicates all of said m object circuits pass said test, in case

that all of m said test circuit output signal indicate that said first data is coincident with said reference data.

43. (previously presented) The testing circuit according to claim 38, wherein said total judgment result signal indicates at least one of said m object circuits fails said test, in case that at least one of m said test circuit output signal indicates that said first data is not coincident with said reference data.

44. (previously presented) The testing circuit according to claim 38, wherein said block judging unit includes:

n individually judging units, each of which compares one of n bits of said first data with corresponding one of n bits of said reference data, and outputs a comparison result as a comparison result signal, and

a second logical processing unit which outputs said block judgment result signal indicating whether or not said first data is coincident with said reference data, based on a plurality of said comparison result signals supplied from said n individually judging units.

45. (previously presented) The testing circuit according to claim 44, wherein said block judgment result signal indicates that said first data is coincident with said reference data, in case that all of said comparison result signals indicate that said one of n bits of the first data is coincident with said corresponding one of n bits of the reference data.

46-74. (cancelled)